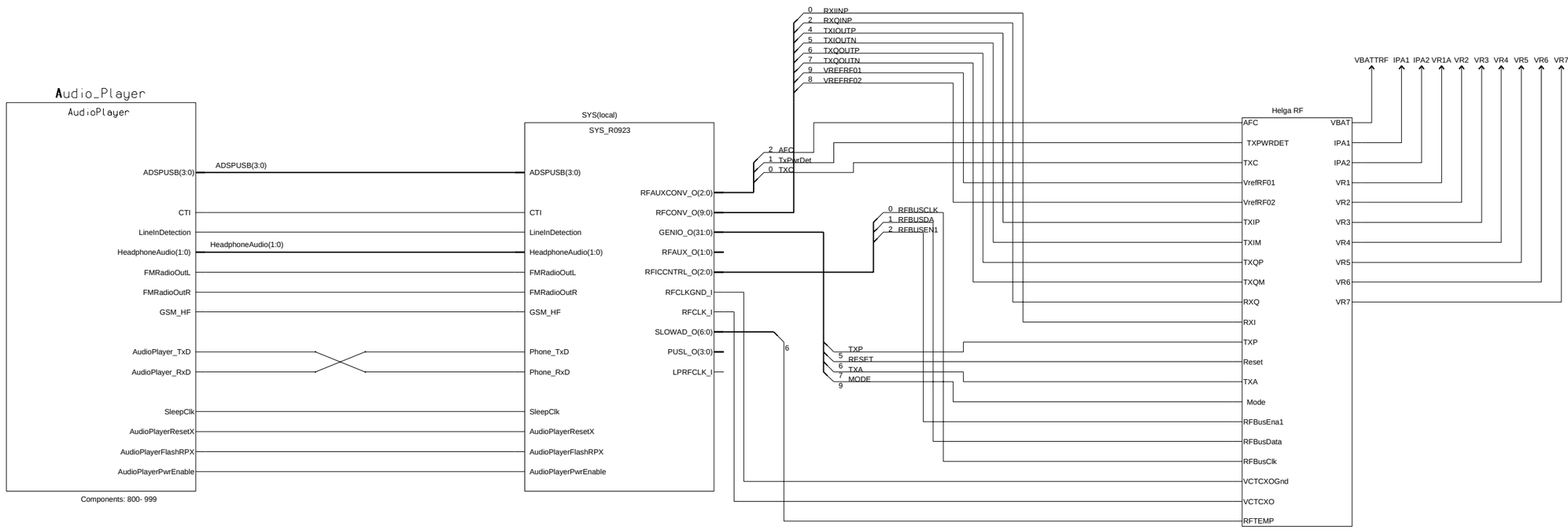
Top sheet (ver.01 ed.41



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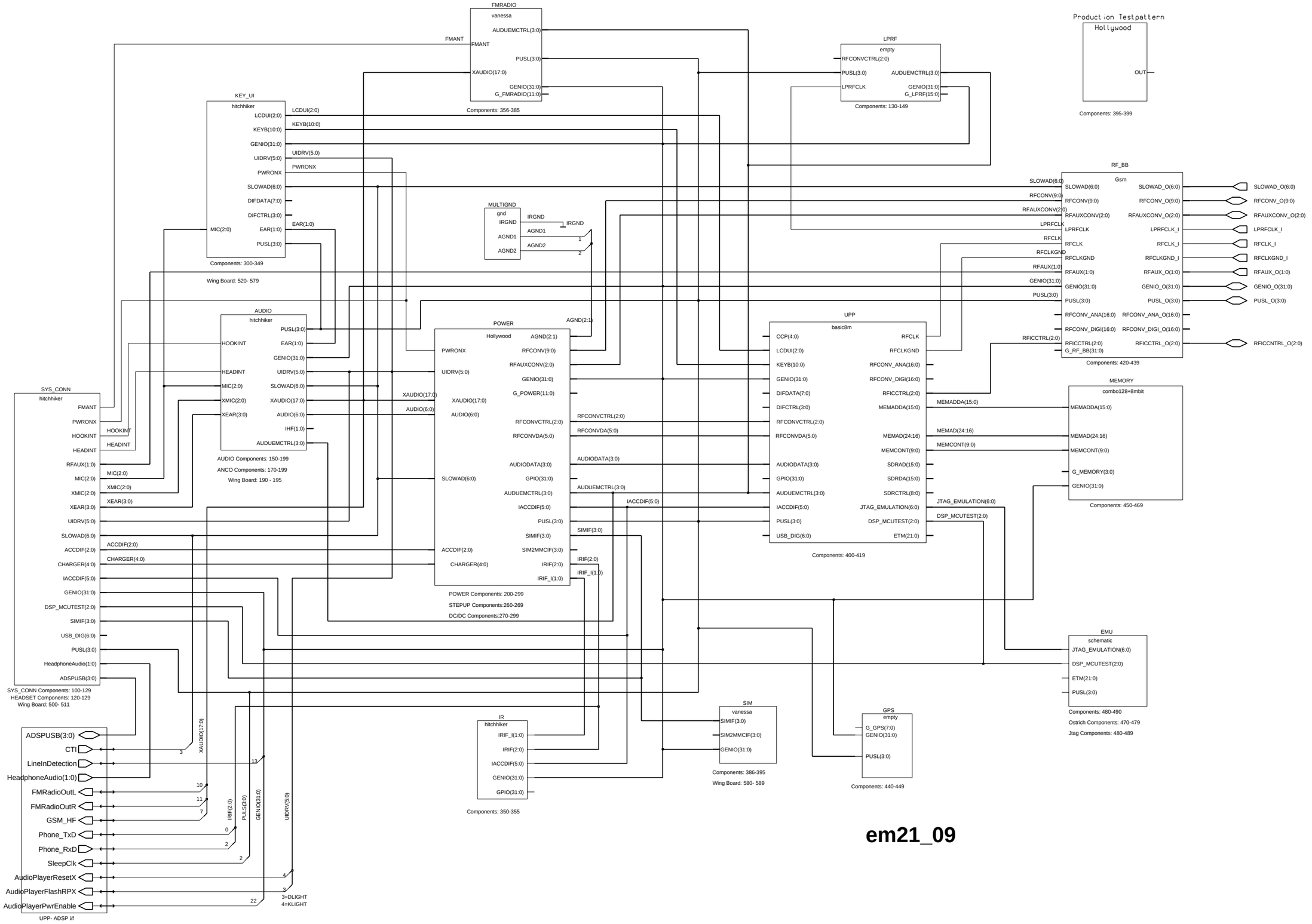
DCT4 common baseband (v.0.0 ed 2)



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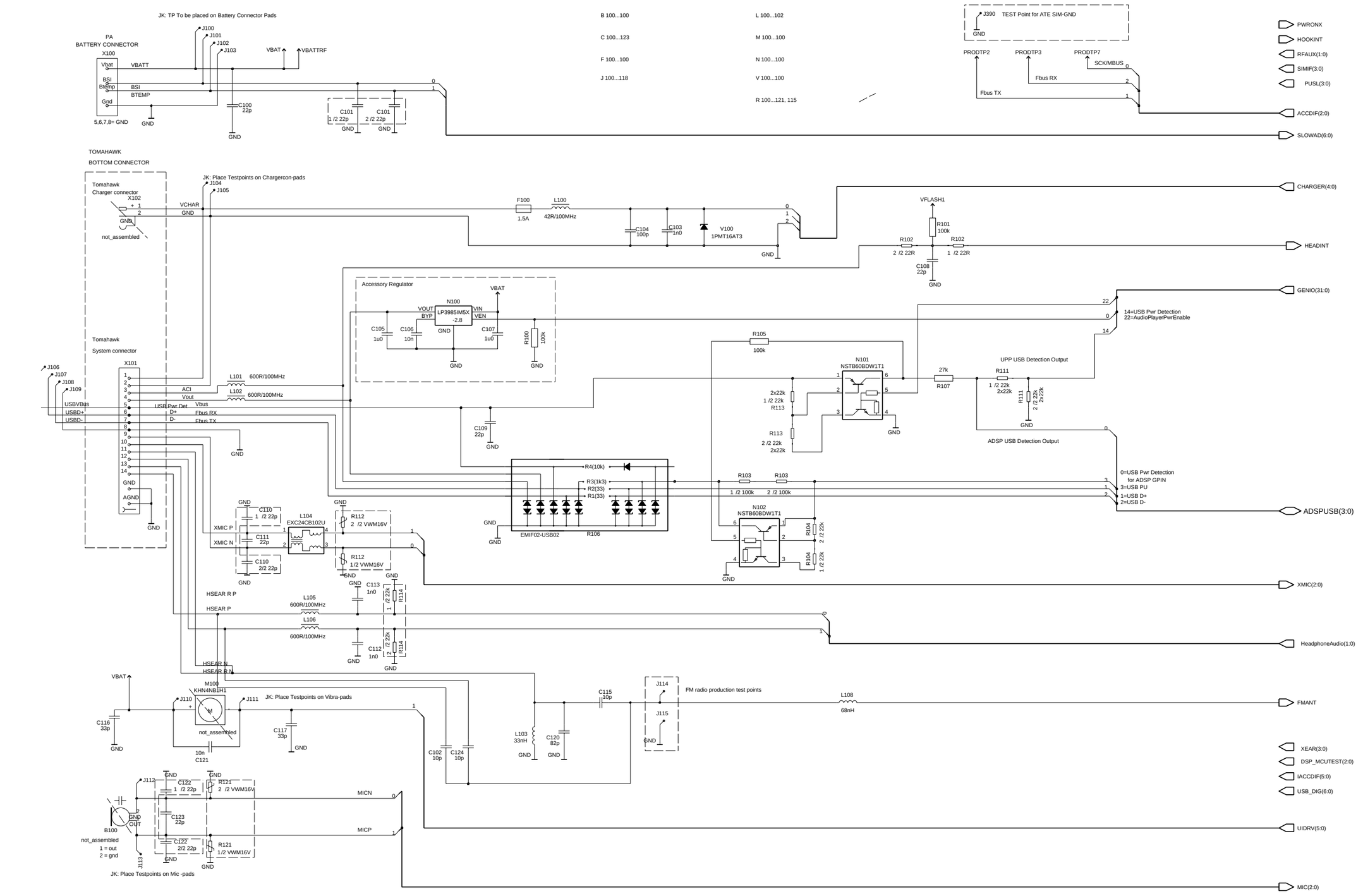
System Connector



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Key user Interface

L 300...300 R 300...314

N 300...300 S 300...303

C 300...305 V 300...305

G 300...300 X 300...301

PUSL(3:0)

MIC(2:0)

DIFDATA(7:0)

DIFCTRL(3:0)

UIDRV(5:0)

0=BUZZO
1=VIBRA
2=CALLED1
3=DLIGHT
4=KLIGHT
5=CALLED2

VBAT

N301
TK11851L
U//U
EN Vin Cx Is GND EXT Vfb Vovp

C300 1u0 GND

C301 33p GND

L300 22uH

V301 STPS0520Z

C302 1u0 GND

R304 39R GND

LCDUI(2:0)

VIO VFLASH1

X300

GND

LCDUI_0
LCDUI_1
LCDUI_2
GENIO_4

LED+
LED-
LED1-
LED2-
DC-OUT_VDD
DC-OUT_CTI

GENIO_24
GENIO_21
GENIO_25
GENIO_27
GENIO_28

R307 1k0 not final
R308 1k0

B2B_Connector_1

B2B connector
pin sort in Layout

1 2
3 4
5 6
* *
21 22

SLOWAD(6:0)

VBACK

G300 3V3 SMD backup battery

GND

GENIO(31:0)

PWRONX

C306 22p
100R R311
R313 1.4V/46V

READ COMPONENT INFO!
G300

POWER

R315 100k
R312 2 /2 VWM16V
G301

Volume up

R316 100k
R312 1 /2 VWM16V
G302

Volume down

R314 1.4V/46V
G303

hotkey

X301

GENIO 2

KEYB(10:0)

EAR(1:0)

B2B_Connector_2

B2B connector
pin sort in Layout

1 2
3 4
5 6
* *
21 22

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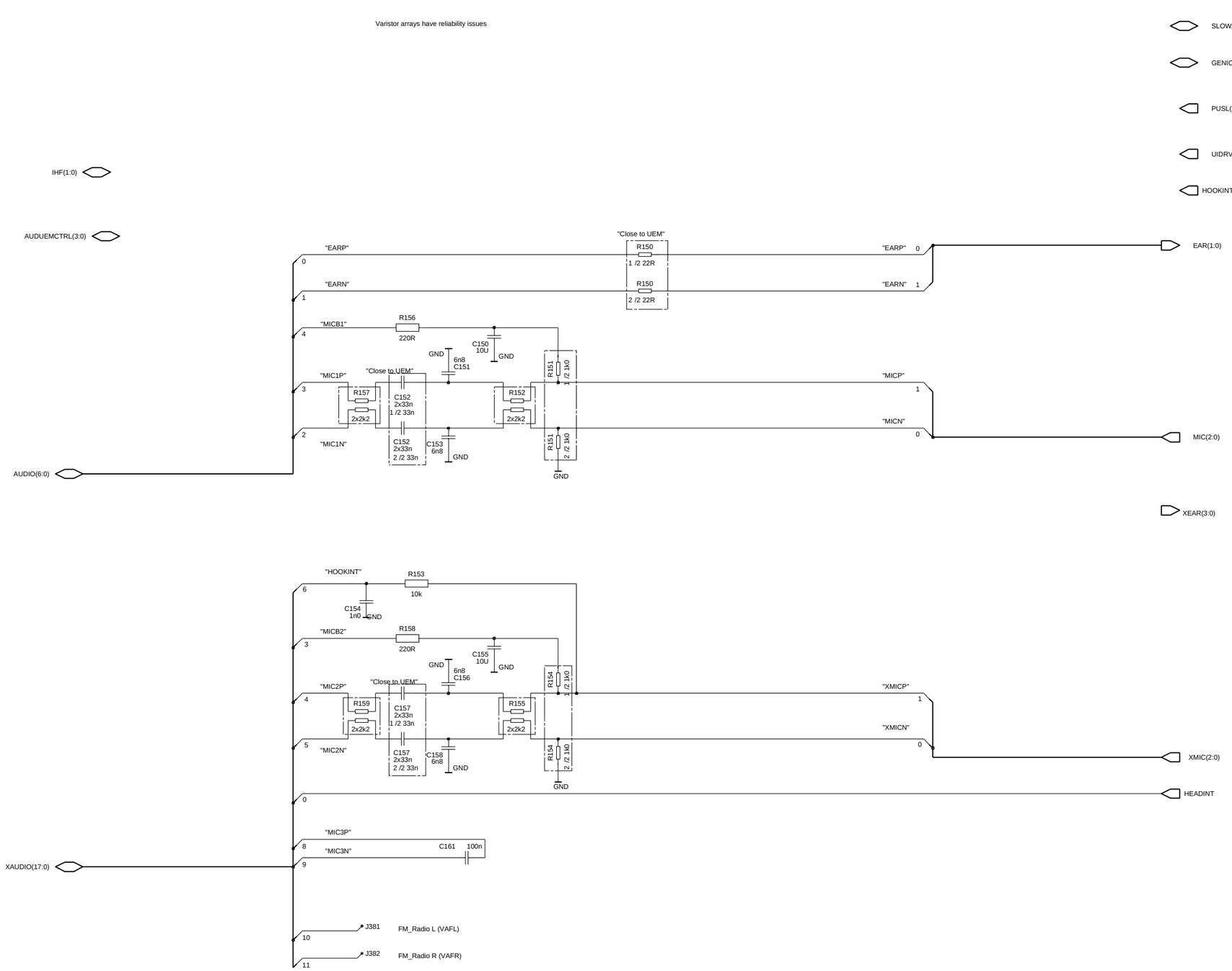
Audio

R 150...155

C 150...160

Varistor arrays have reliability issues



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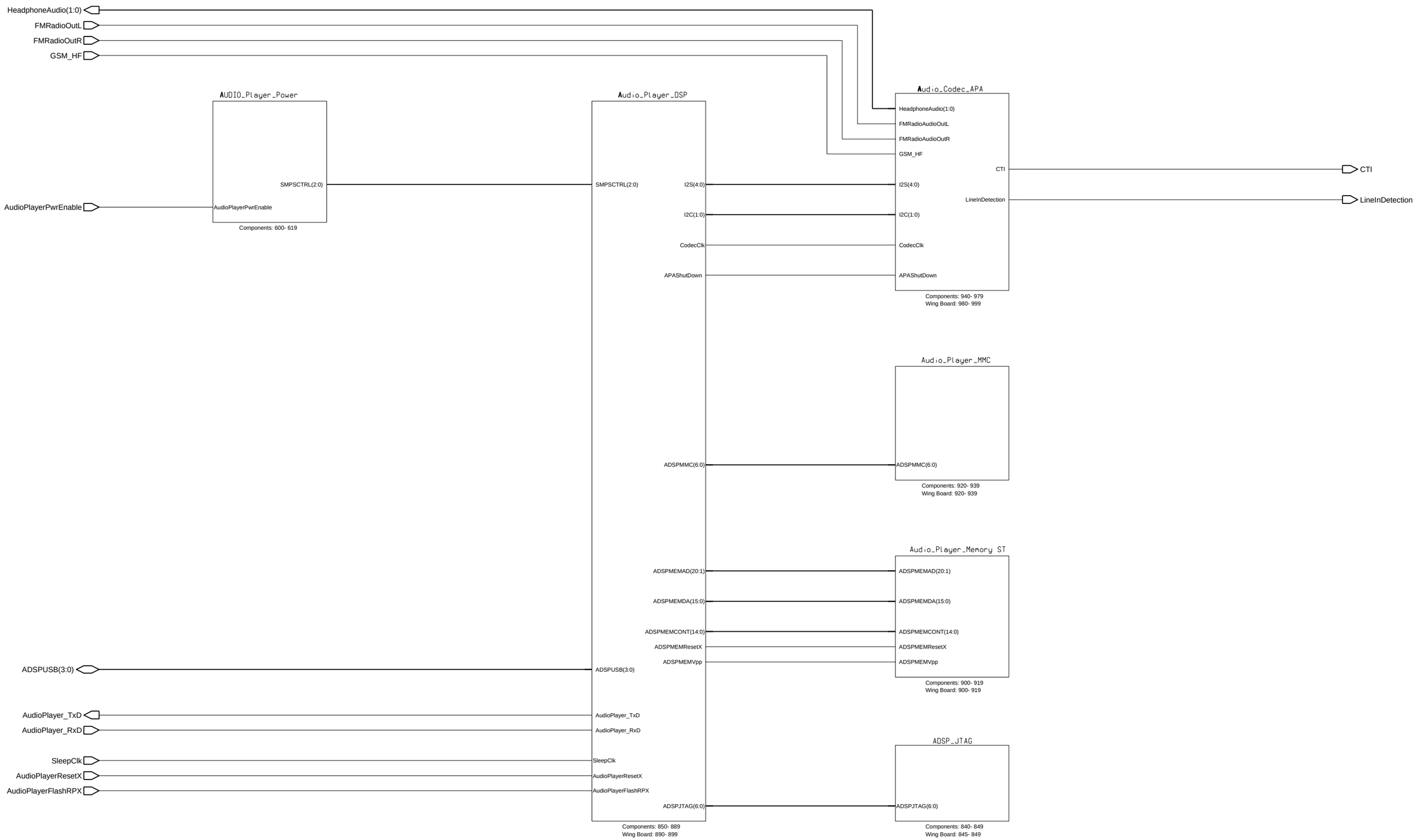
Audio player



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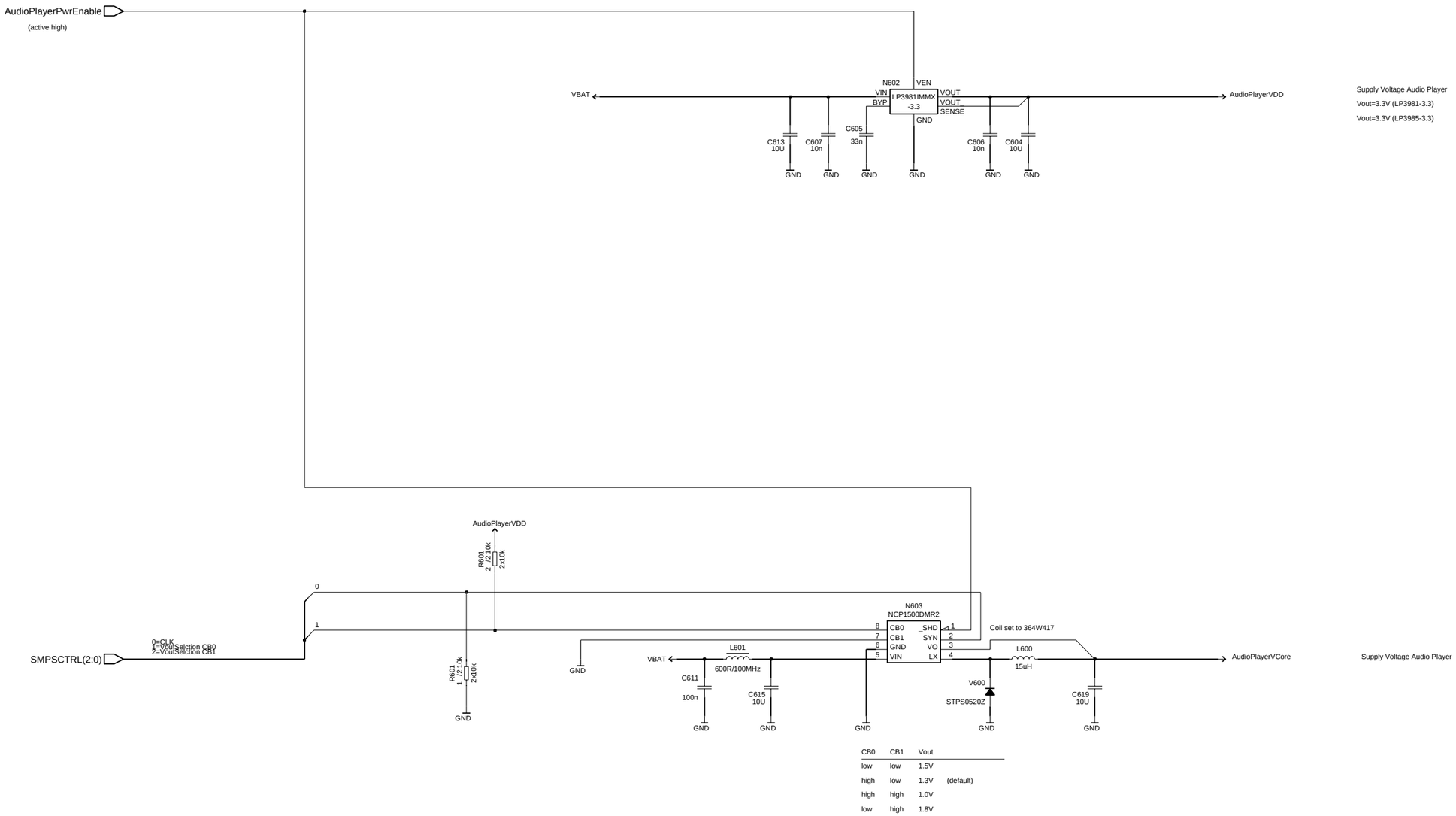
Audio Power



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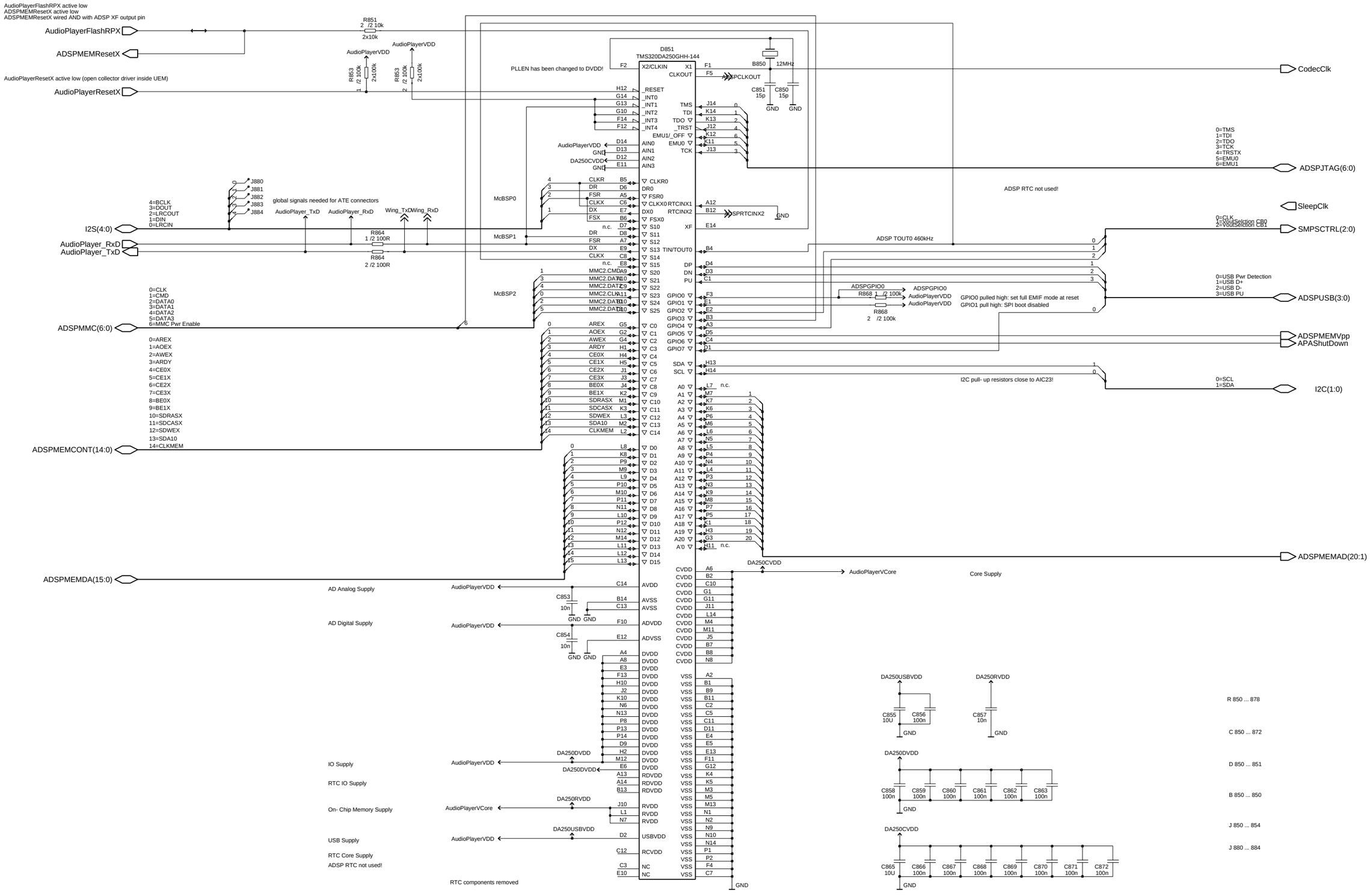
Audio DSP



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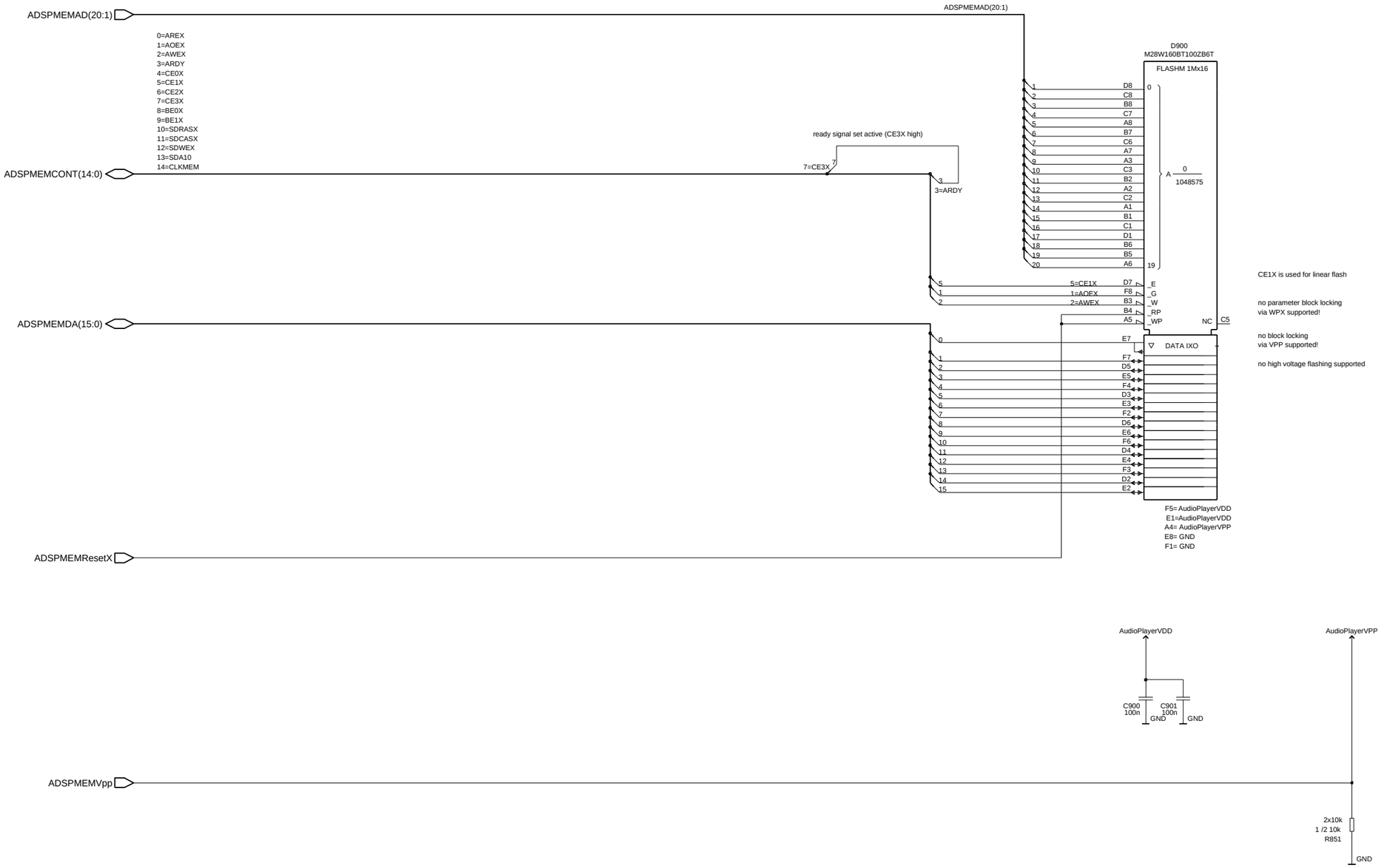
Memory ST



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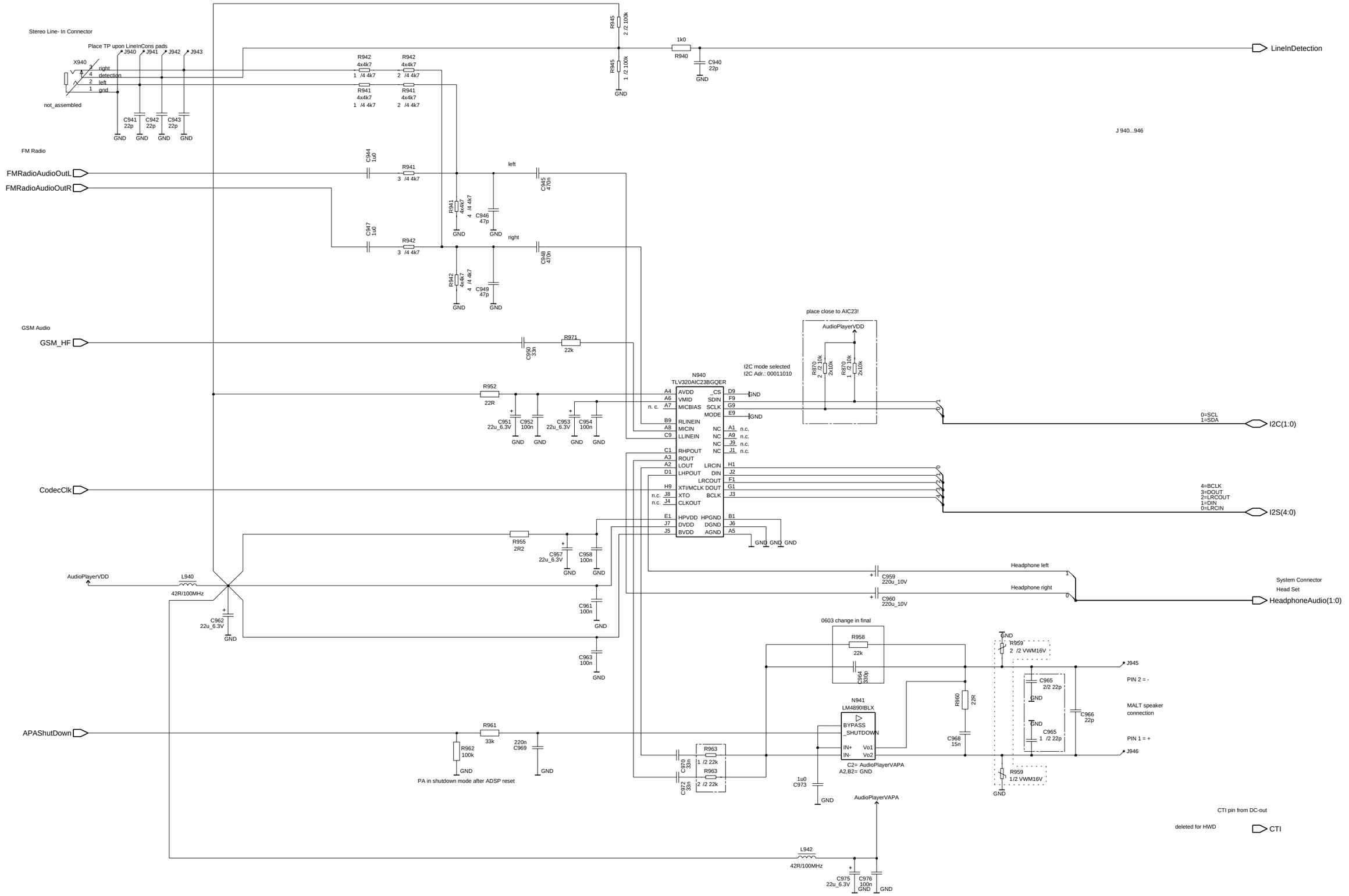
Audio Codec



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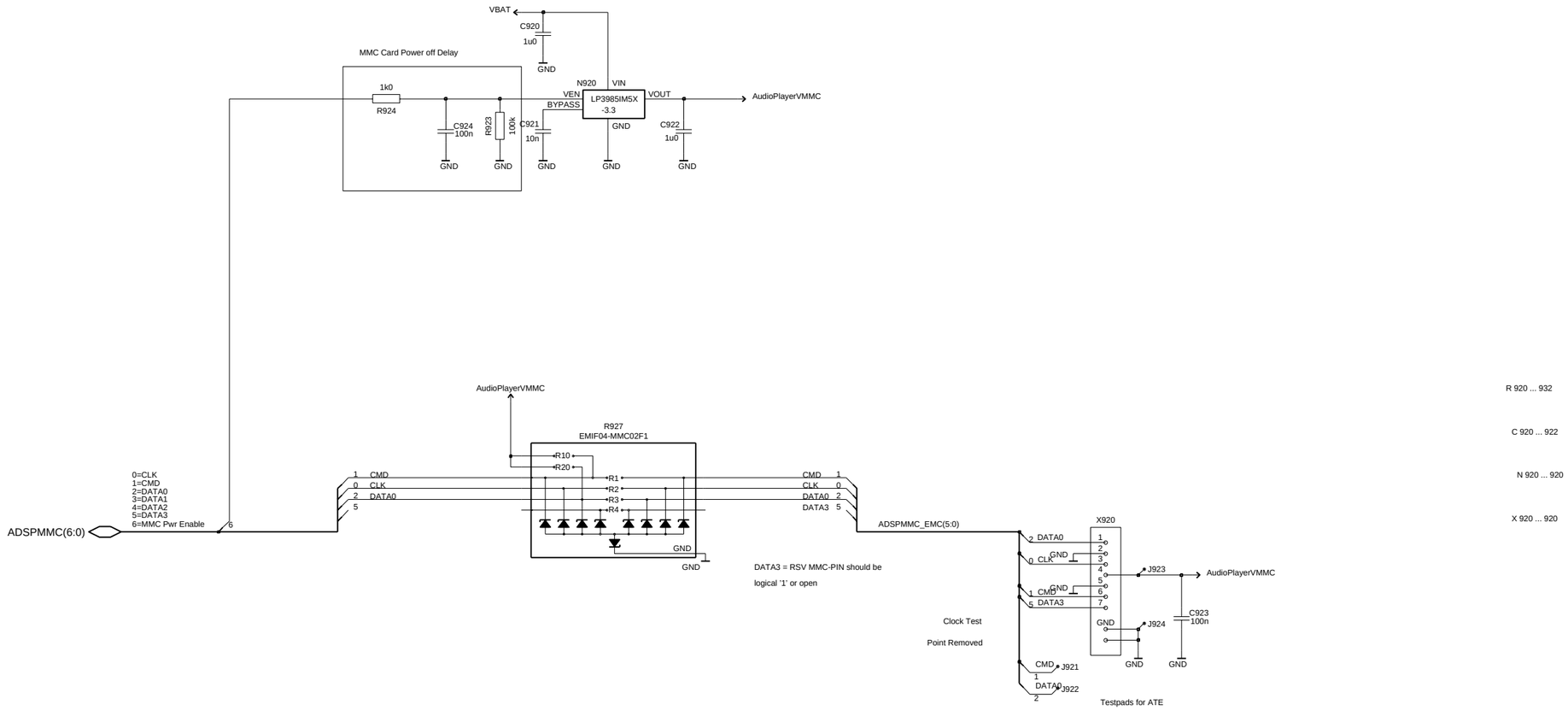
´MMC



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JTAG interface

ADSPJTAG(6:0)

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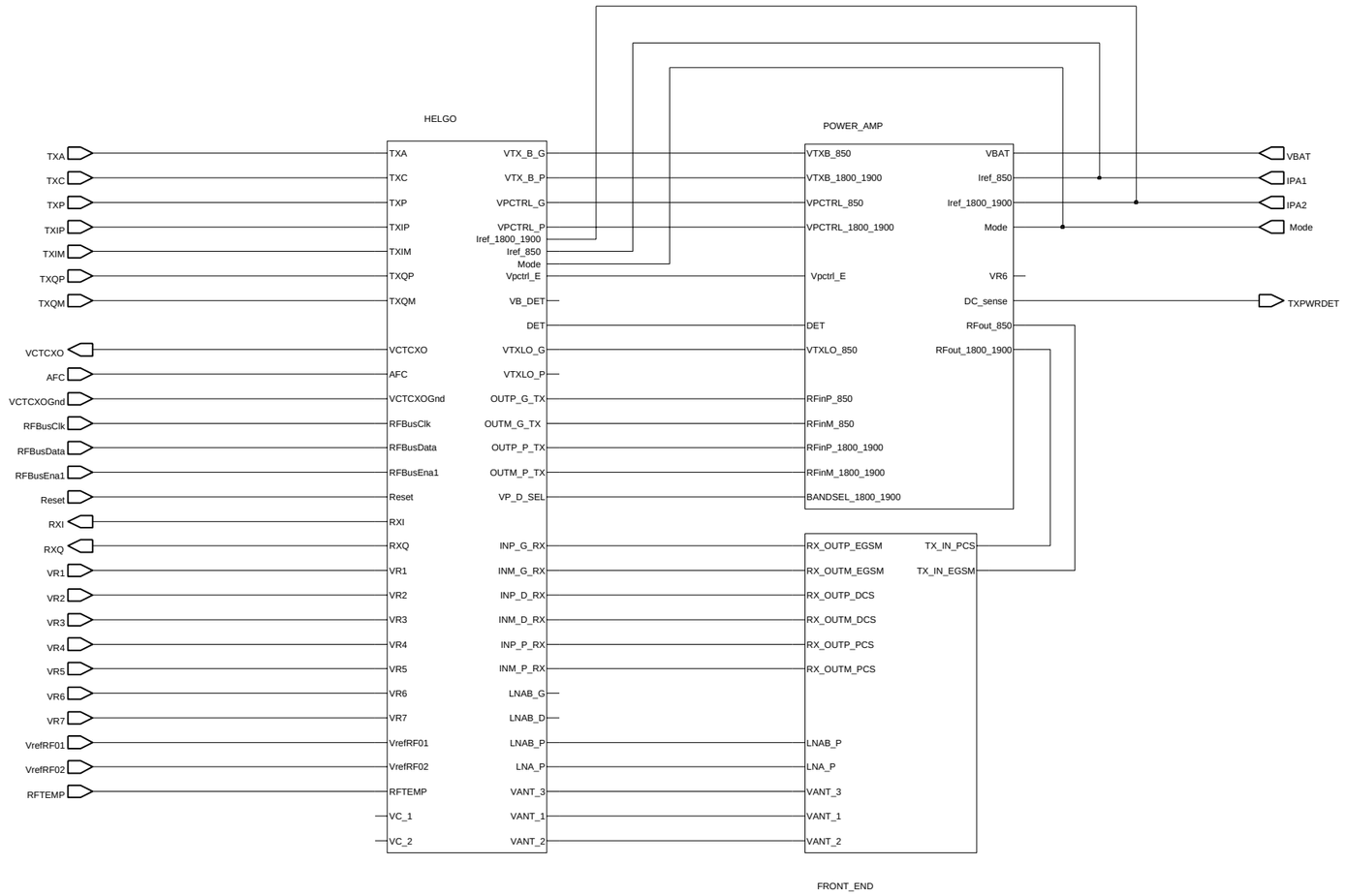
RF block diagram



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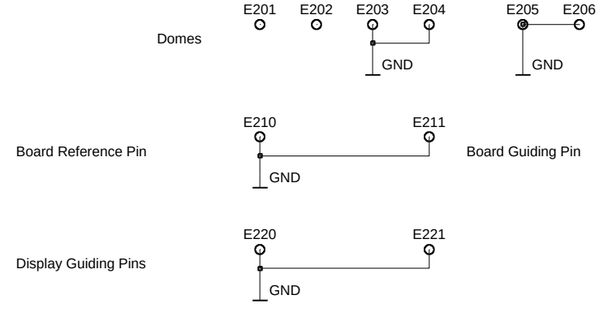
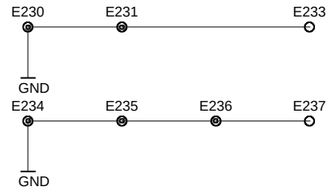
RF grounds

RF GLOBAL GND HOLES

SYSTEM GLOBAL GND HOLES



Acoustic holes



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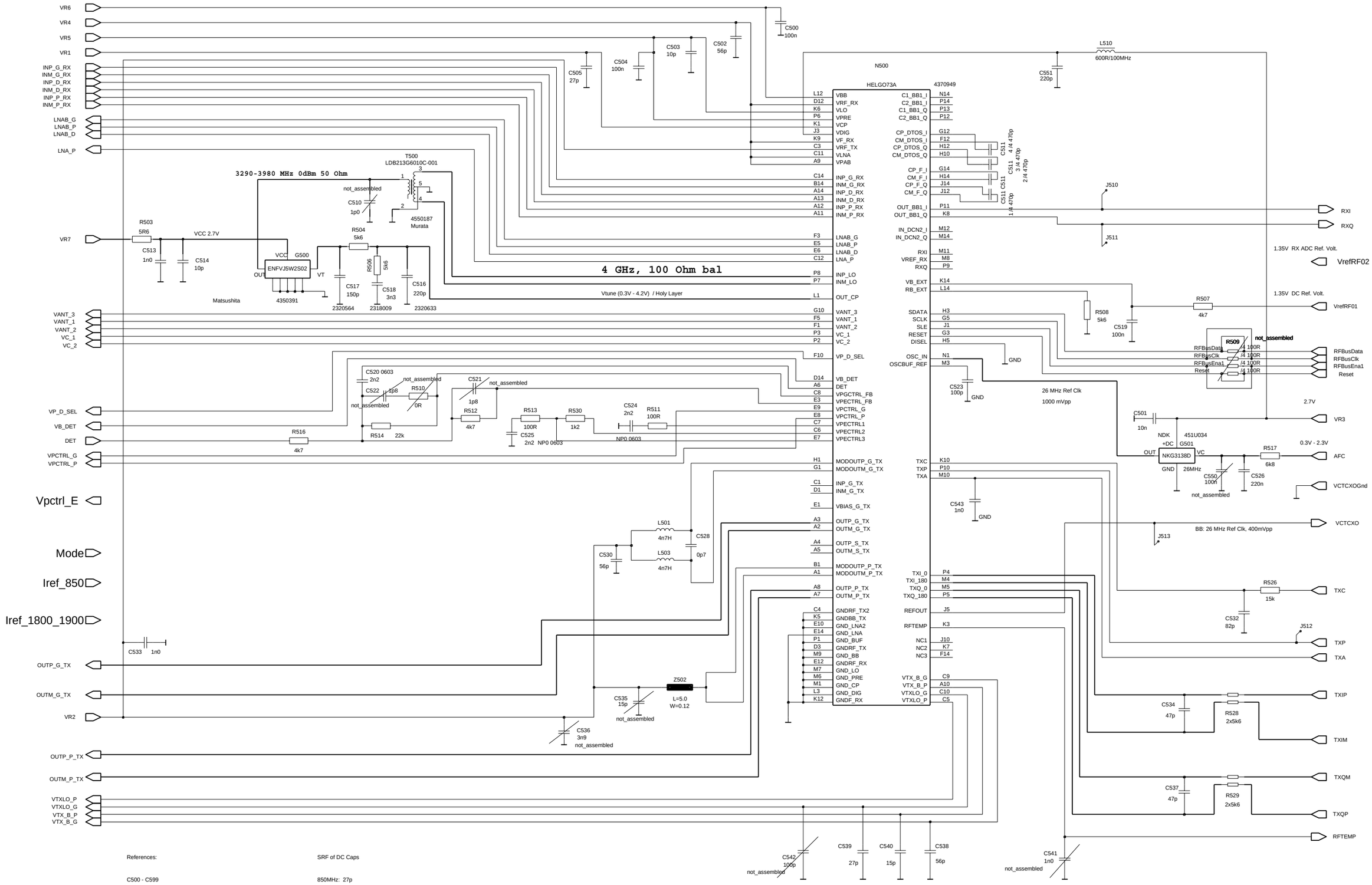
HELGA ASIC



References:

C500 - C599

R500 - R599

L500 - L599

G500 - G599

SRF of DC Caps

850MHz: 27p

1900MHz: 15p

3600MHz: 10p

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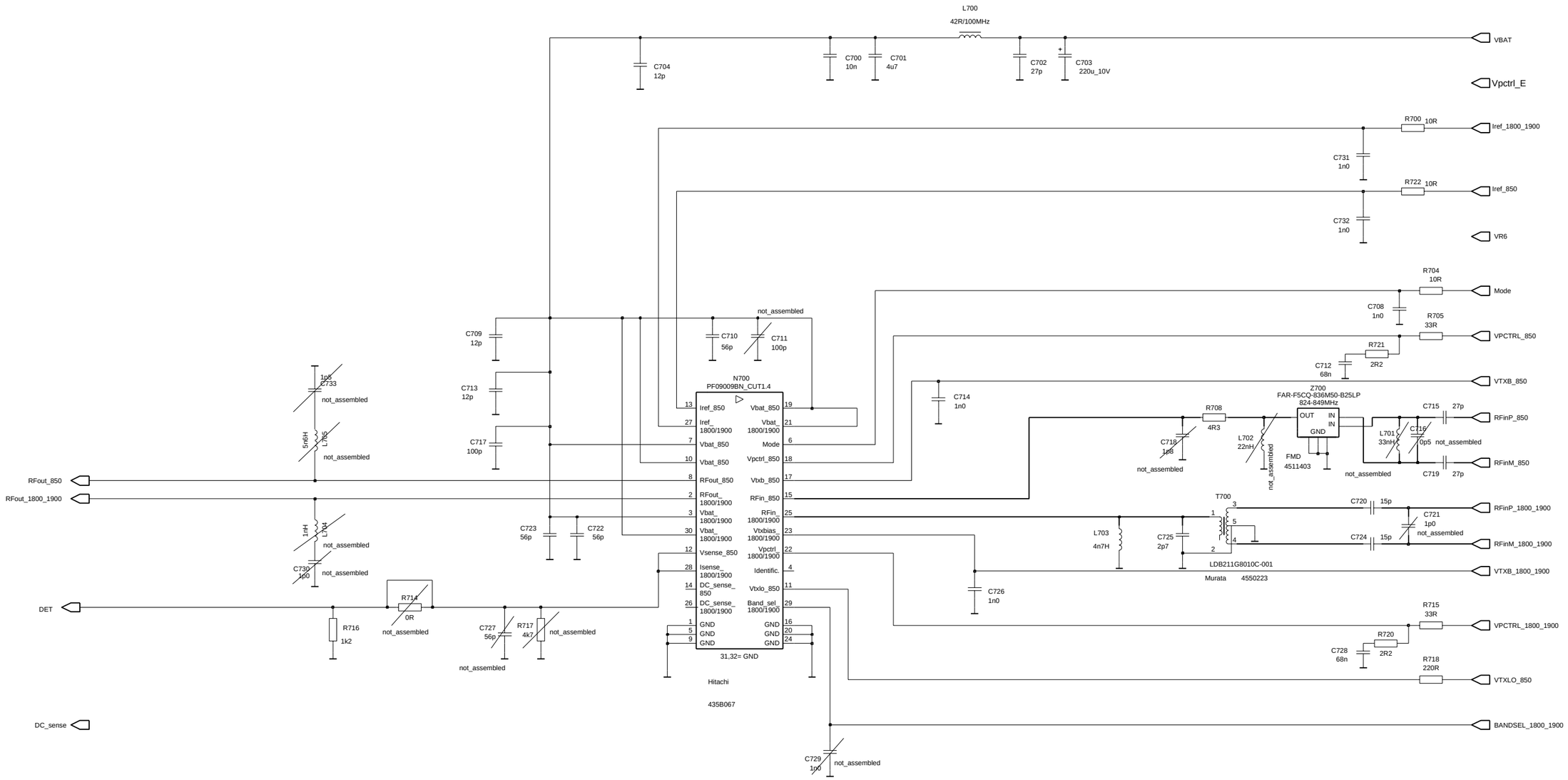
Power amplifier and detection



References:

C700 - C749	SRF of DC Caps
R700 - R749	850MHz: 27p
L700 - L749	1900MHz: 15p
Z700 - Z749	

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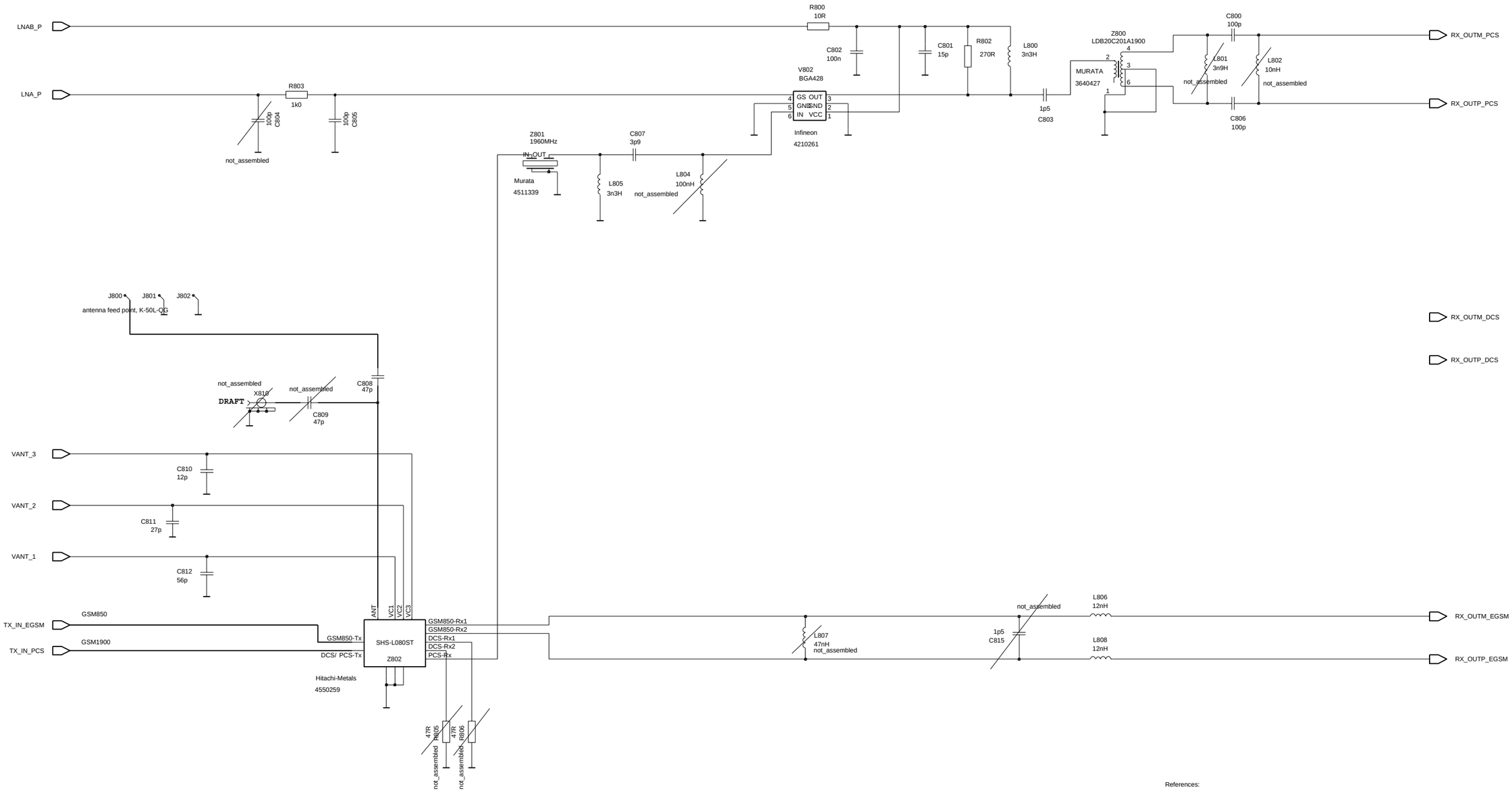
RX front end and antenna switch



References:

C800 - C849

R800 - R849

L800 - L849

Z800 - Z849

SRF of DC Caps

850MHz: 27p

1900MHz: 15p

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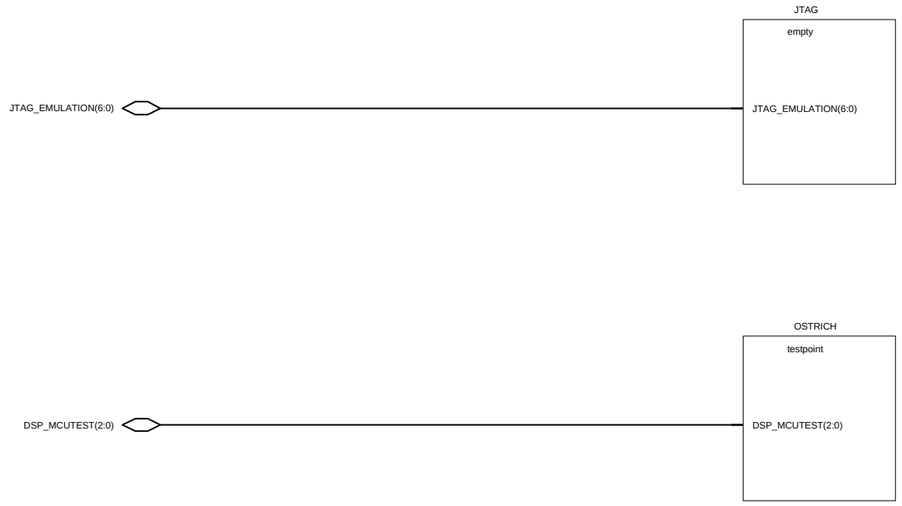
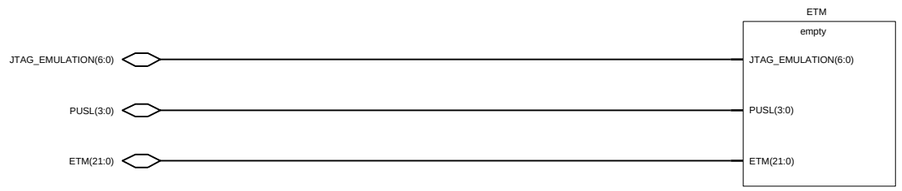
Test and emulator interface





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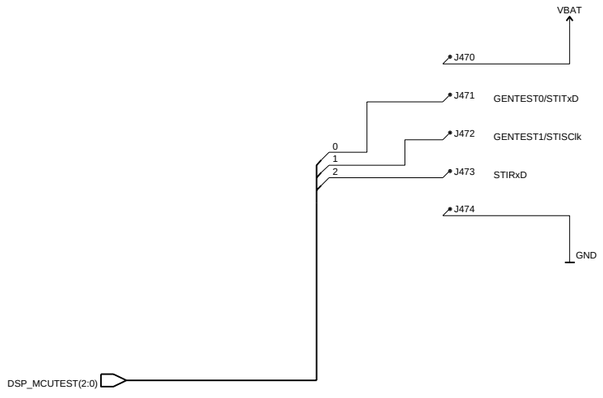
Testpoints



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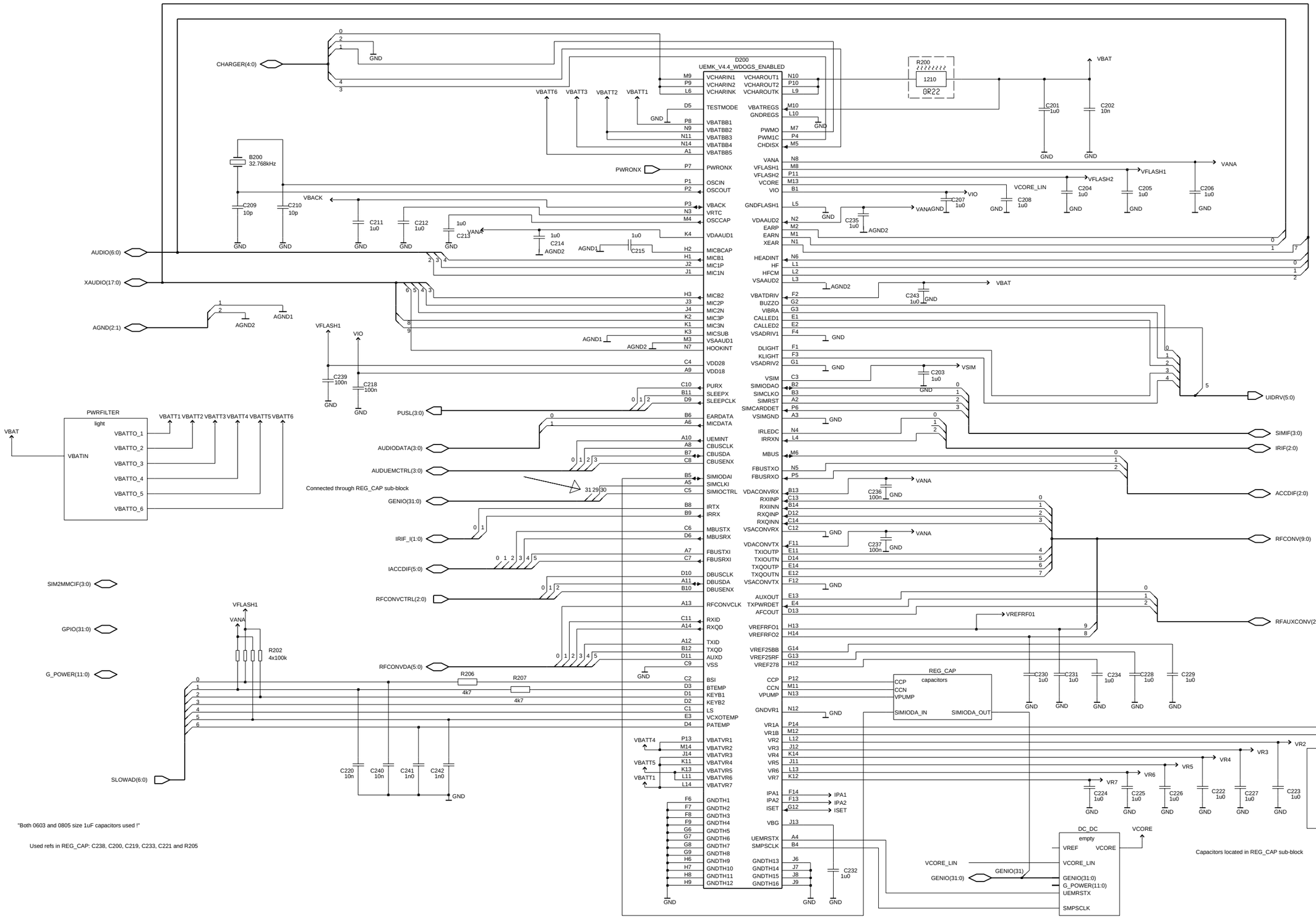
Discrete power management



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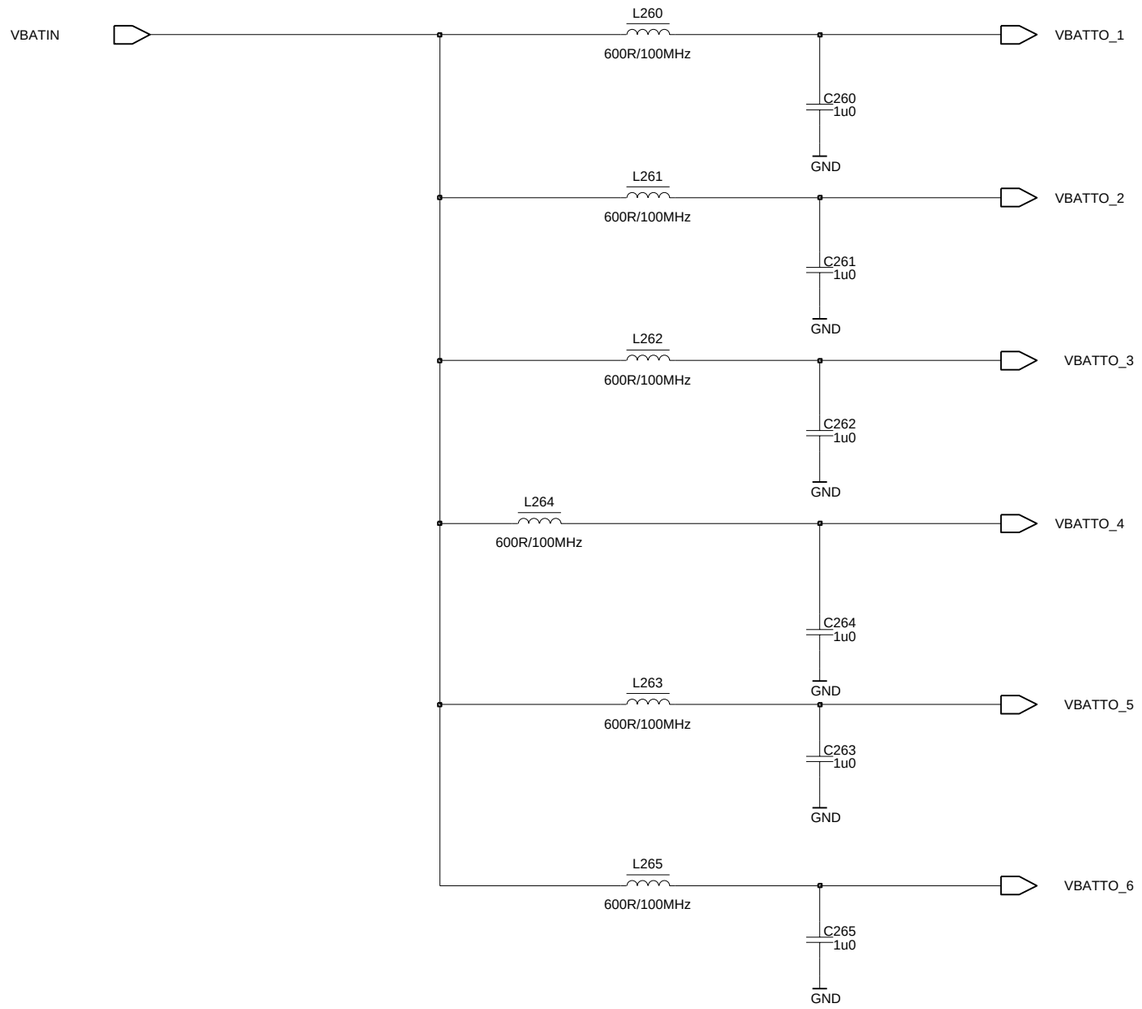
Light filtering



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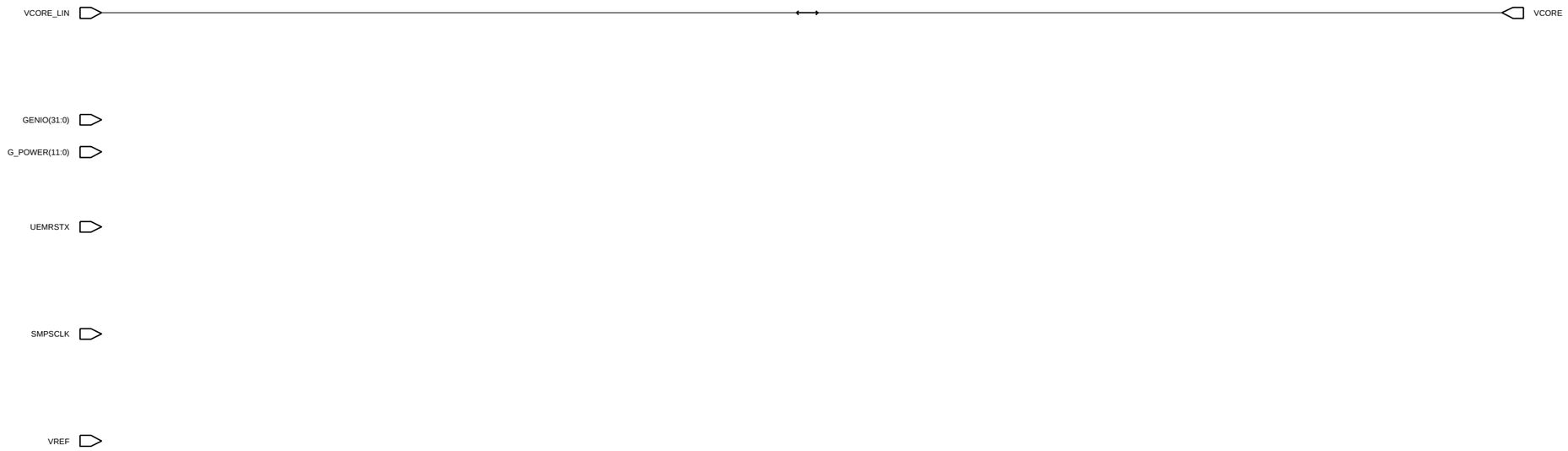
DC/DC converter



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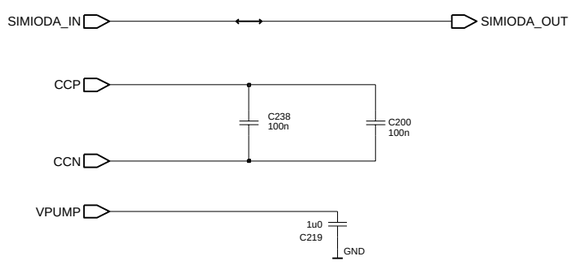
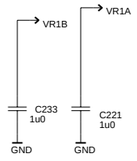
Old power discrete





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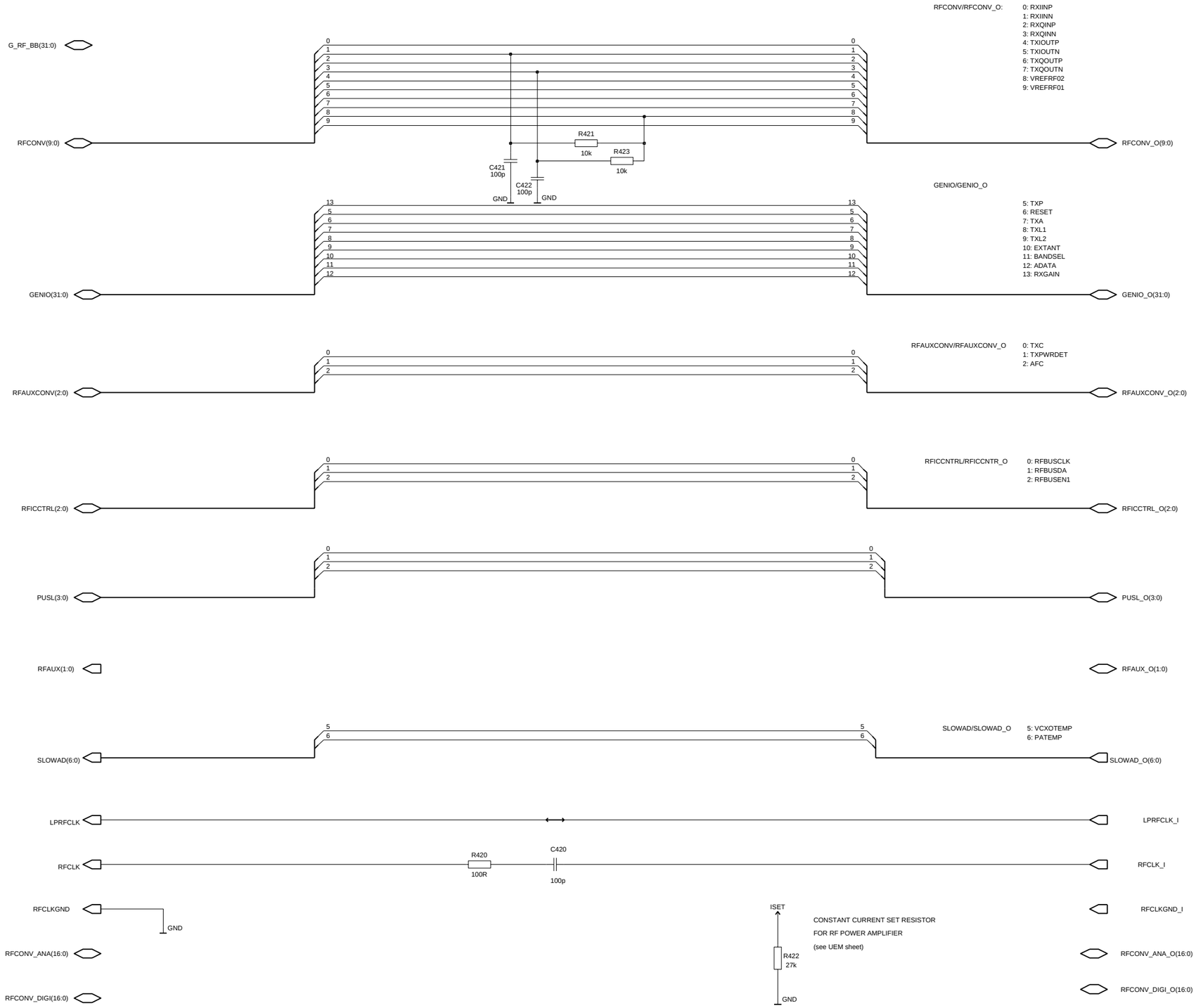
GSM RF and BB interface



IF IPA1 AND IPA2 ARE USED BY RF THE TOLERANCE HAS TO BE 1% (0402, 1430873)

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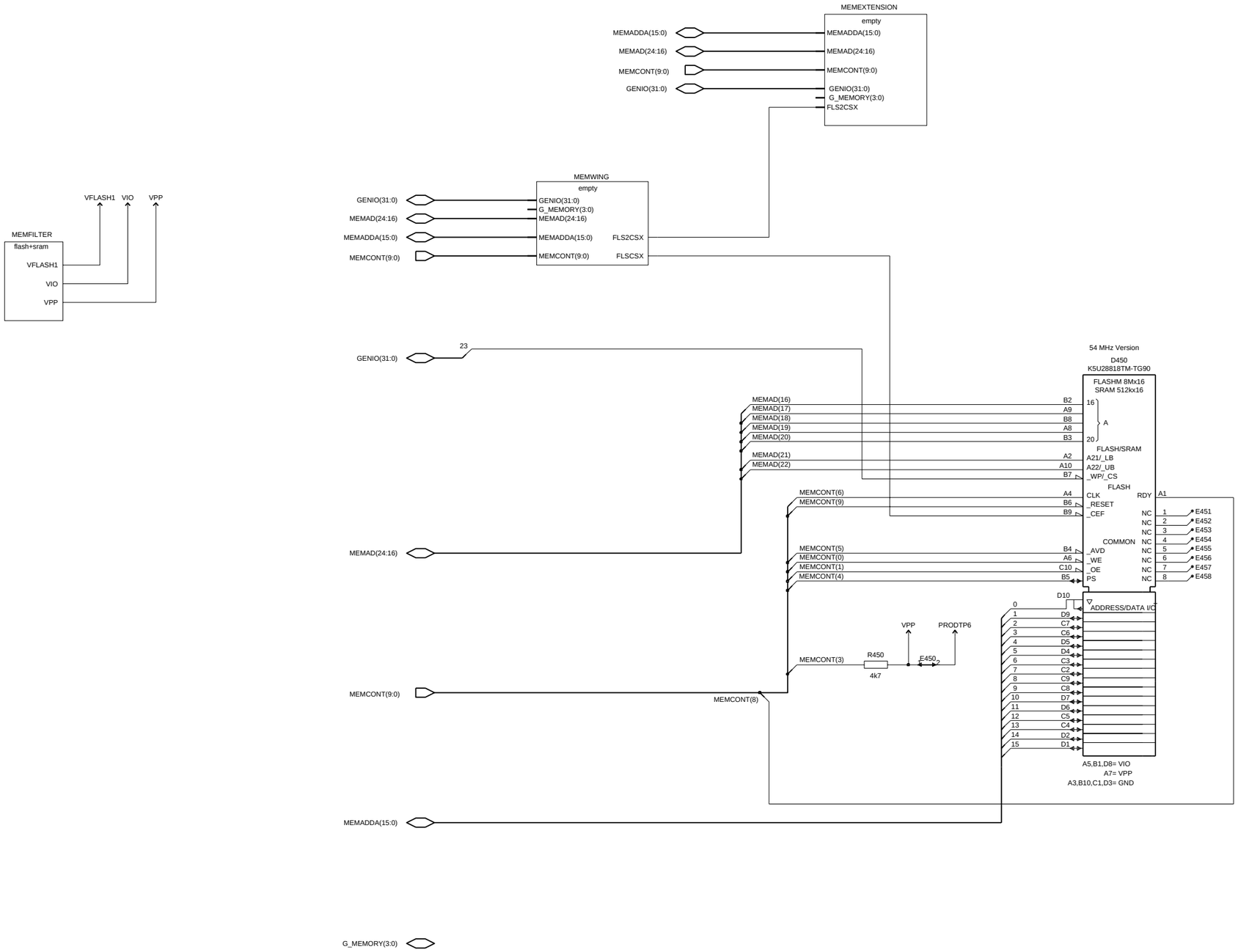
Combo memory



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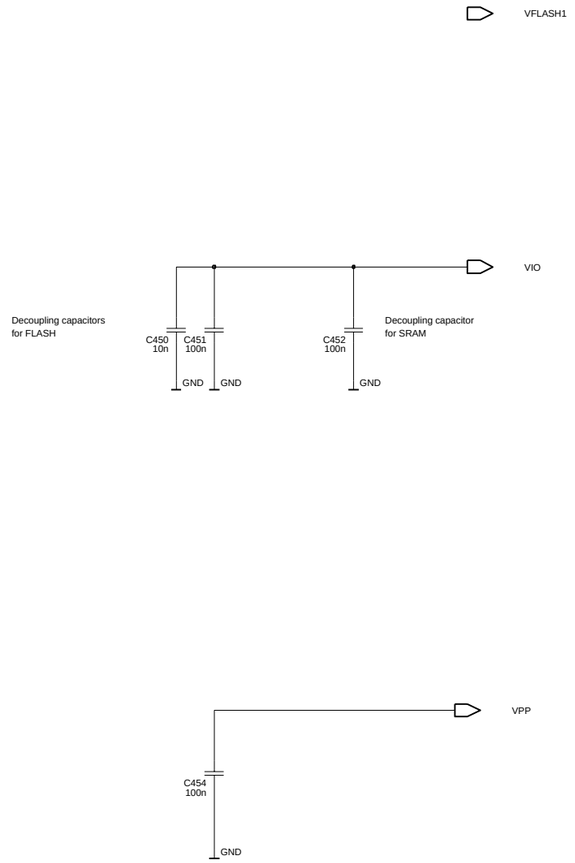
Decoupling capacitators for Flash and SRAM



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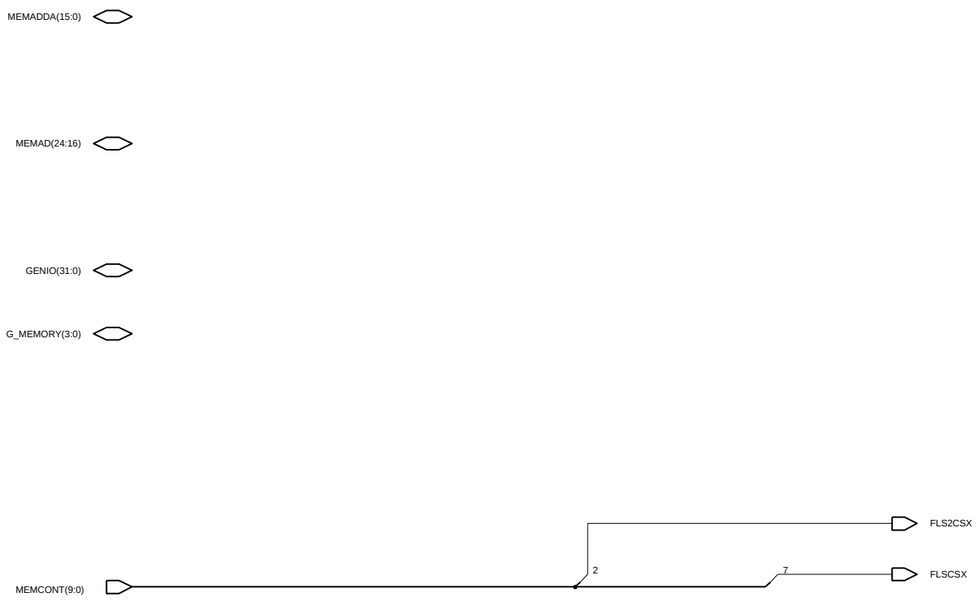
Empty wing sheet



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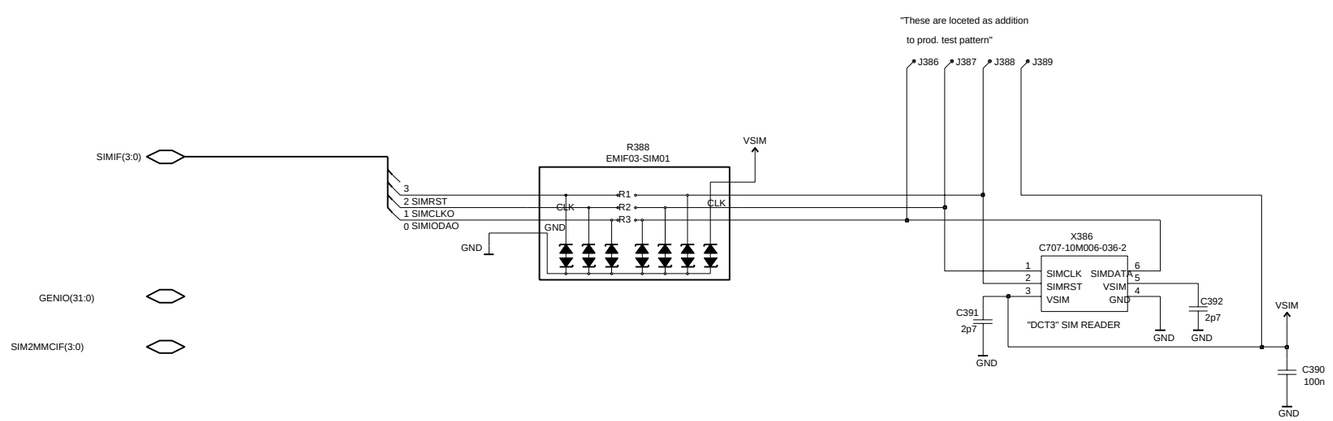
SIM reader



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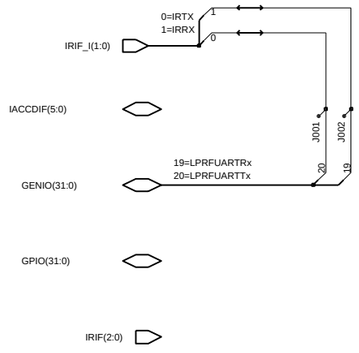
Application engine interface



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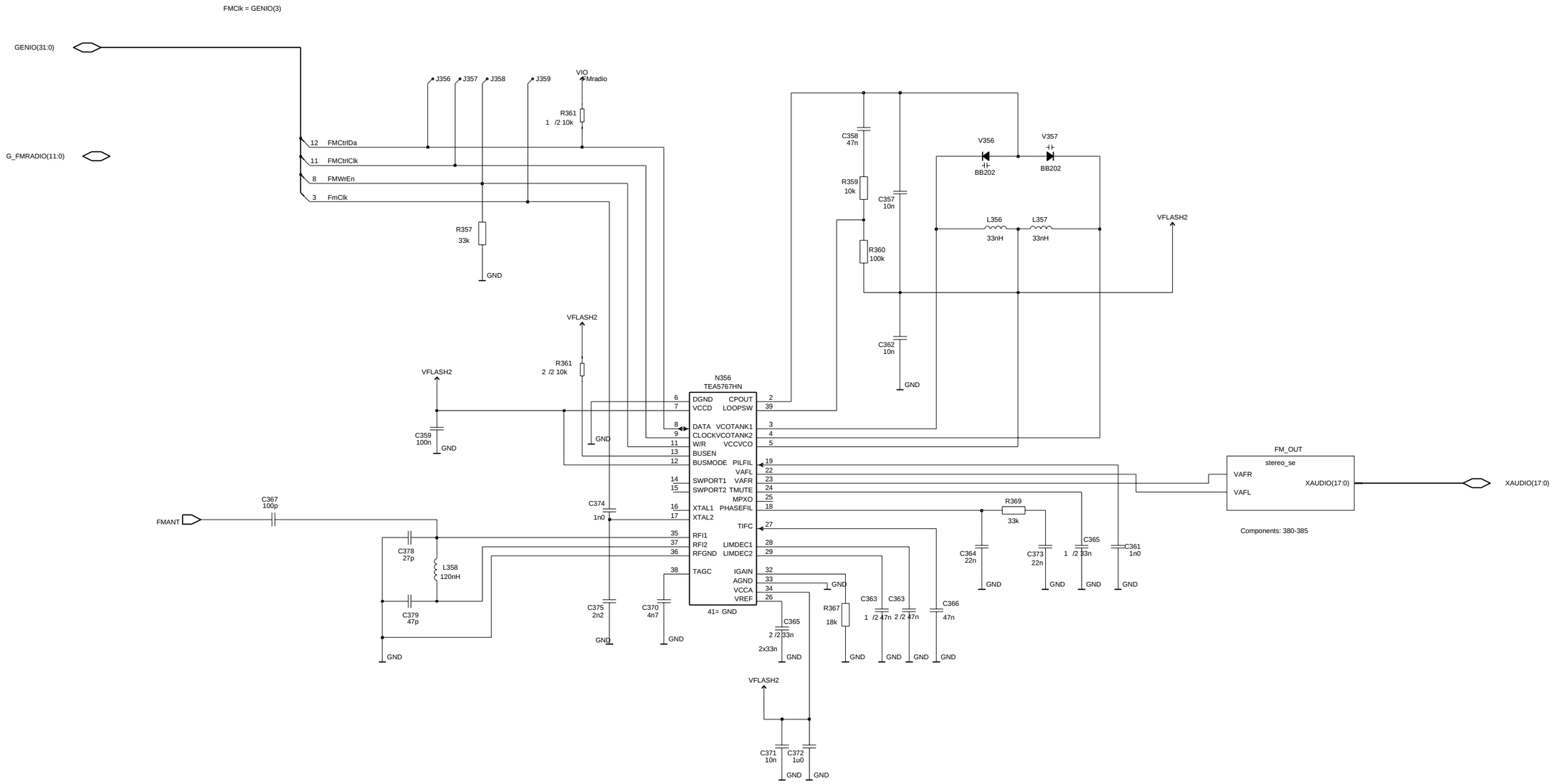
FM Radio



Notice:

C374 (1n0) and C375 (2n2) are configured for 32kHz reference clock

If reference clock is 6.5MHz, use C374 (3p9) and C375 (10p)

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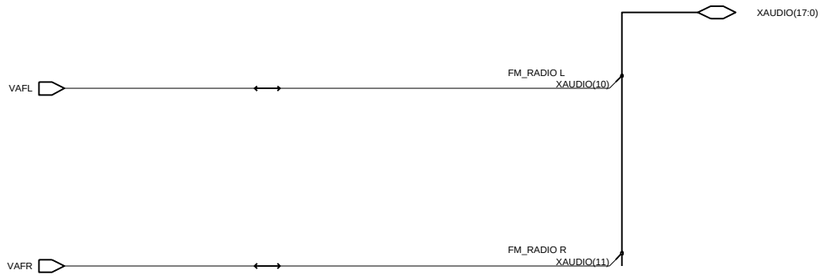
FM Radio



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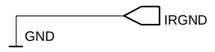
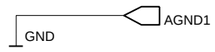
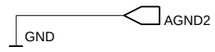
Multi GND







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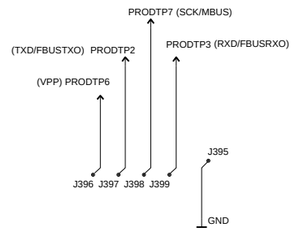
5 pin production test pattern

OUT



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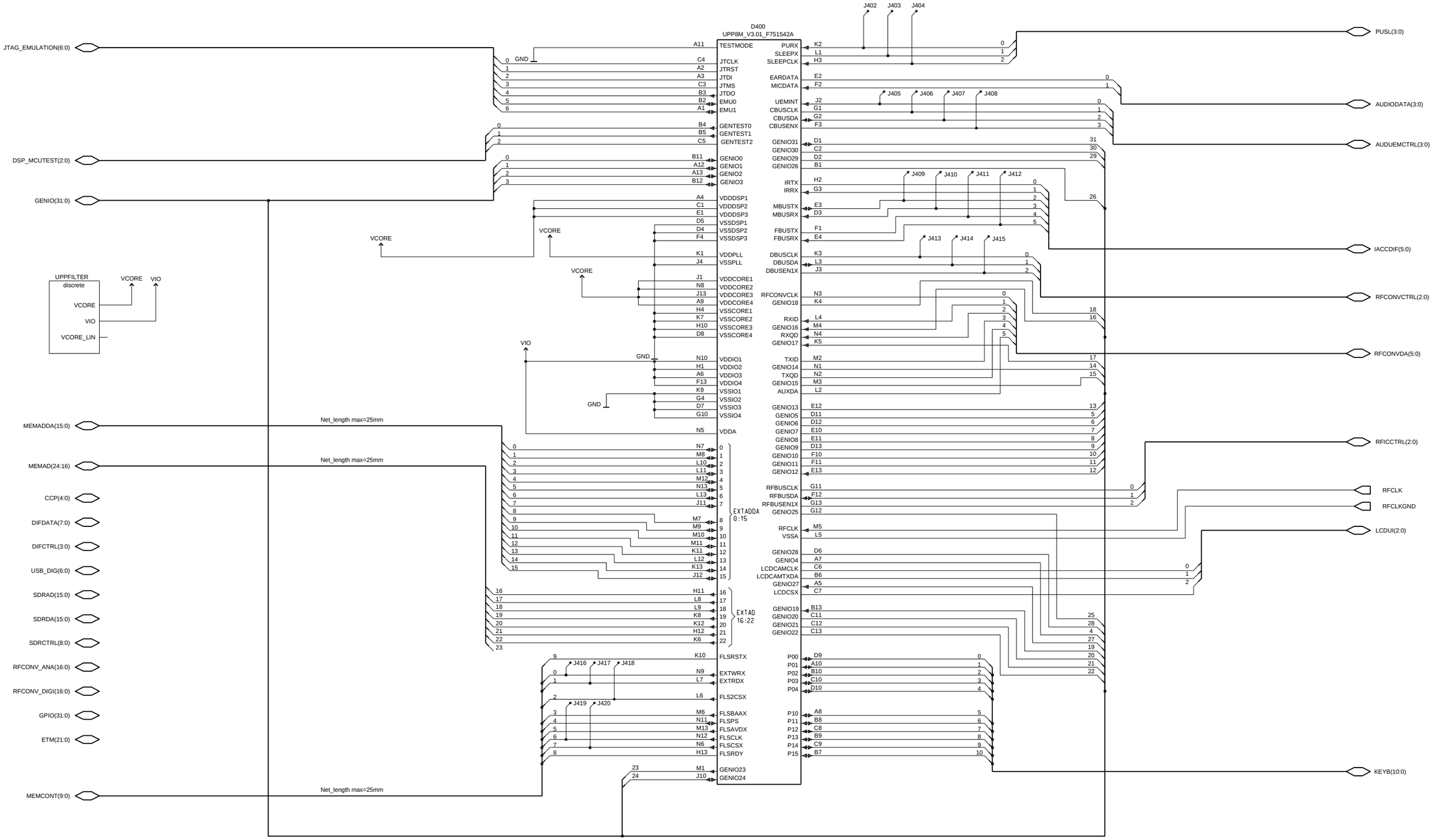
UPP 8M



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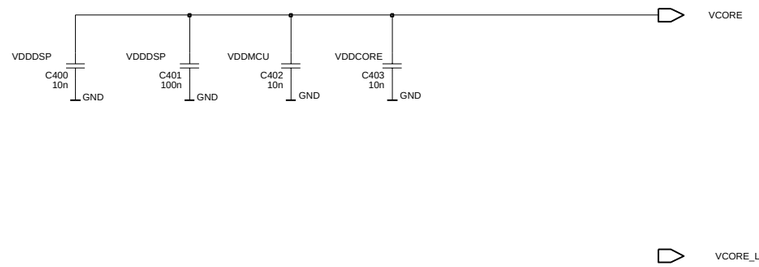
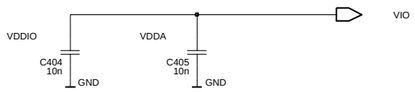
Discrete decoupling capacitators for UPP





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